Integration of Single-Walled Carbon Nanotubes on to CMOS Circuitry with Parylene-C Encapsulation

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***Abstract*- This paper presents heterogeneous integration of Single-Walled Carbon Nanotubes (SWNTs) with CMOS integrated circuits using die-level post processing. The chip was fabricated using the AMI 0.5µm CMOS Technology. An electroless zincation process was performed over the Aluminum assembly electrodes (Metal 3 of CMOS technology) to clean and to coat the electrodes with a thin Zinc layer. Low temperature dielectrophoretic assembly was utilized for the placement of the SWNTs on to these electrodes. Encapsulating the CMOS chip with a thin (1µm) parylene-C layer stabilized the SWNT-electrode contact resistance and also provided environmental protection. Electrical measurements from the assembled SWNTs yield ohmic behavior with a two-terminal resistance of ~44KΩ. The SWNTs were incorporated on to the CMOS chip as a feedback element of a two-stage Miller compensated high gain operational amplifier. The measured small signal ac gain (~1.95) from the inverting amplifier confirmed the successful integration of carbon nanotubes with the CMOS circuitry. This paper lays the foundation for the realization of next generation integrated nanosystems with active nanostructures on CMOS integrated circuits.**

Keywords-CMOS circuitry; Dielectrophoretic assembly; Nano scale integration; Parylene-C encapsulation; Single-Walled-Carbon-Nanotubes (SWNTs).

I. INTRODUCTION

Single-Walled Carbon Nanotubes (SWNTs) have been attracting substantial interest as potential building blocks of chemical and biological sensors and future integrated circuits. [1, 2]. SWNTs are graphene cylinders with a wall thickness of one atomic layer and a diameter of about one nanometer. They have very exciting properties such as high aspect ratio, large surface area and hollow geometry [3], high current carrying capacity, superior thermal properties, fast response and good reversibility [4, 5]. These properties present nanotubes as viable candidates for sensing applications, such as gas sensors [6], pressure sensors [7], transistors [8, 9], and thermal sensors [10, 11].

Despite the initial success in implementing nanotube based sensors, the integration of nanotubes onto CMOS electronics is nascent. Recently, catalyst based CVD growth and AFM-assisted alignment are utilized for realizing SWNT based devices. However, the high CNT growth temperatures (~700°C) are not compatible with CMOS technology [12, 13]. The technique of AFM-assisted CNT placement is fairly difficult to control and is impossible to scale up to volume manufacturing [14, 15]. The heterogeneous integration of nanostructures with CMOS circuitry has numerous advantages: reduced parasitics due to the absence of wire bonding, higher sensor sensitivity through on chip signal processing, and low-cost miniaturized system-on-chip solutions. Historically, utilizing the materials provided by CMOS technology allowed the realization of various integrated micro systems. Moreover, depending solely on CMOS technology has limitations specifically in the availability of materials. [16].

There have been numerous approaches developed to incorporate nanoscale materials on to microdevices. One such technique, Dielectrophoretic (DEP) assembly, classified as a bottom-up approach, is a versatile and low temperature technique to manipulate nanoscale materials [17-19]. In DEP assembly, a nonuniform electric field is generated by the application of an AC voltage, and the nanomaterials suspended in a solution are attracted to regions where the intensity of the field is either maximum (positive DEP) or minimum (negative DEP). Furthermore, DEP assembly is a simple, low cost, and wafer scale process which is compatible with CMOS technology. Previously, Close and coworkers have utilized DEP assembly and have demonstrated MWNT interconnect lines using a relatively complicated post-CMOS approach [20]. In order to isolate the circuitry from the assembly voltage, they first conducted the DEP assembly and then etched the assembly electrodes and connected their CNTs to the circuitry. Furthermore, Chow and coworkers have designed and fabricated a CNT-CMOS low-power sensor chip [21].

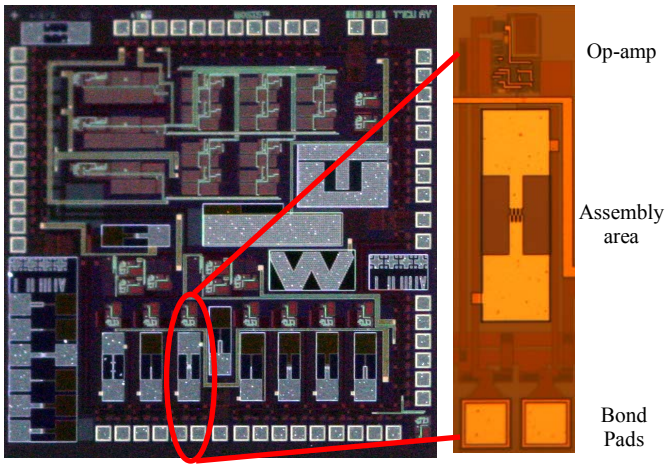

Fig. 1 Optical photograph of the CMOS chip.

However, a relatively high AC voltage (20 V_{pp}) was utilized during the DEP assembly which was not compatible with CMOS circuitry. To address this problem, proper design of the electrodes and the circuitry is needed.

In this paper, we present heterogeneous integration of Single-Walled Carbon Nanotubes on to a CMOS chip (Fig.1) utilizing low voltage DEP assembly. The integration of the nanotubes is achieved using a DEP process which is low temperature and is suitable for wafer scale manufacturing. The presented technique is versatile and can be utilized for the realization of numerous nanomaterial based systems fabricated on CMOS circuitry.

II. Experimental Details

The CMOS chip comprising of the electrodes for the assembly of SWNTs and the interface circuitry was designed and fabricated using the AMI 0.5µm CMOS process, provided by MOSIS. SWNTs were assembled on to the electrodes realized by the top metal layer (M3) using Dielectrophoresis. Dielectrophoresis is an inexpensive and high yield method for manipulation, trapping, and separation of micro- and nanomaterials and is utilized in these work. The integration of SWNTs on to CMOS circuitry was realized utilizing a post-CMOS fabrication approach which is illustrated in Fig.2 and is described below.

A. Electroless Zincation Process

The unpackaged chips, 2mm × 2mm in size were received from the foundry with an opening in the top passivation layer,

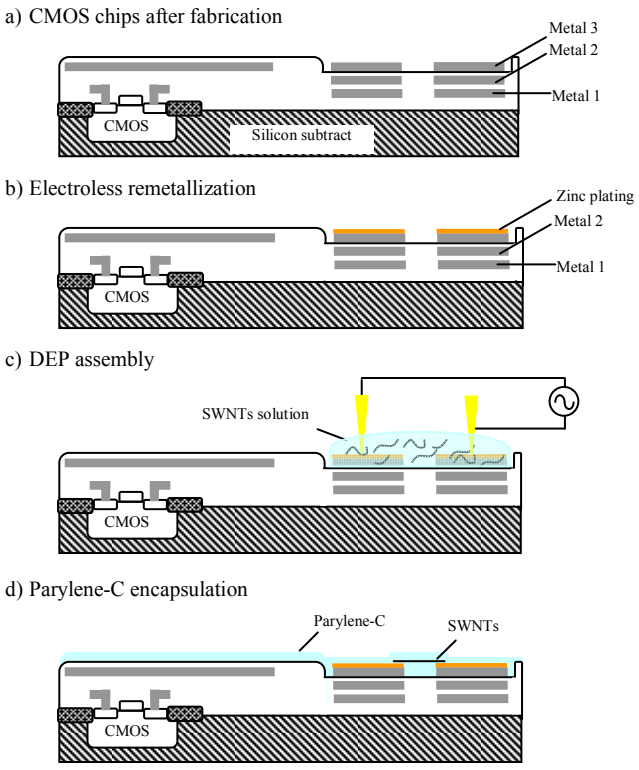

Fig.2 Post-CMOS integration process.

and were mounted on a PDMS/silicon base to facilitate handling. Since the top metal layer of the CMOS chip is made of Aluminum, it readily forms an insulating oxide upon exposure to atmosphere. In order to provide a good contact between the Aluminum electrodes and the SWNTs, an electroless zincation process was performed (Fig.2(b)). It is a selective autocatalytic metal deposition process and a low-cost alternative to vacuum deposition processes and does not require any additional lithography steps. The electroless plating process is fairly straighforward and only requires contact between the aqueous plating solution and the metal lines on the CMOS die [22].

The zincation process started by immersing the CMOS chip in a 1M Sodium hydroxide (NaOH) solution for 2 min to clean the surface of the chip which was followed by a deionized water rinse. Next, the CMOS chip was placed into the zinc plating solution for 2 min which remetalized (with Zinc) the Aluminum electrodes on the CMOS chip. Then, the chip was immersed in 30% Nitric acid (HNO_3) for 15 sec which stripped the granulated initial Zinc deposits and which resulted in smoother Zinc layer during the second zincation process. A deionized water rinse followed the second zincation process and completed the electroless zincation process. As shown in Fig.2(b), this was a "displacement reaction" in which the Aluminum ions were replaced by the zinc ions, thus forming a thin zinc layer. This process prevented the underlying Aluminum from getting reoxidized [23] and improved the contact resistance between the assembled SWNTs and the Aluminum assembly electrodes.

B. Dielectrophoretic Assembly Process

After the electroless zincation process, SWNTs were next assembled in between the two Zinc coated metal electrodes. In these experiments, commercially available aqueous suspension of highly purified HIPCo-grown SWNTs were used with a concentration of 0.004g/ml, which was diluted using deionized water. The average diameter of the SWNTs used was about 2nm with an average length of 3µm. A 1µL SWNT solution was first dispensed onto the electrodes of the CMOS chip and then an AC sinusoidal signal of 5V_{pp} at a frequency of 10 MHz (Fig.2(c)) was applied between the electrodes to perform the DEP assembly. After 30 sec of DEP assembly, the solution was blown-dried with a nitrogen gun. We next encapsulated the SWNTs with a thin (1µm) parylene-C layer (Fig.2(d)) with the purpose to provide environmental protection and to stabilize the contact resistance between the nanotubes and the metal electrodes.

III. Results and Discussion

A. SEM Imaging and I-V Characterization

DEP assembly of SWNTs on to CMOS electrodes was achieved with a high yield and a typical assembly area is shown in Fig.3. The insert image shows an enlarged view of the assembled SWNTs connecting two electrodes. Two-

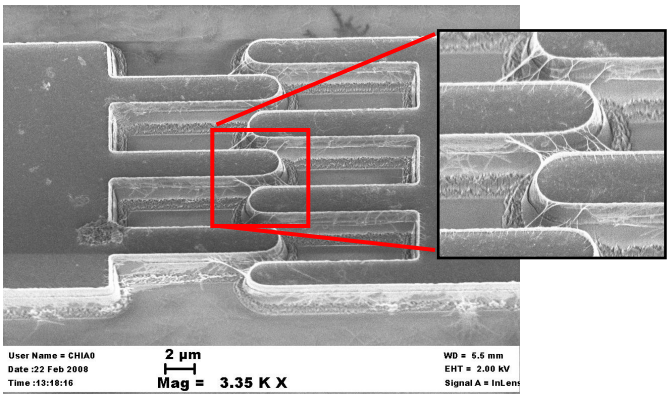

Fig. 3 SEM micrograph of the assembled SWNTs on to microelectrodes connected to CMOS circuitry.

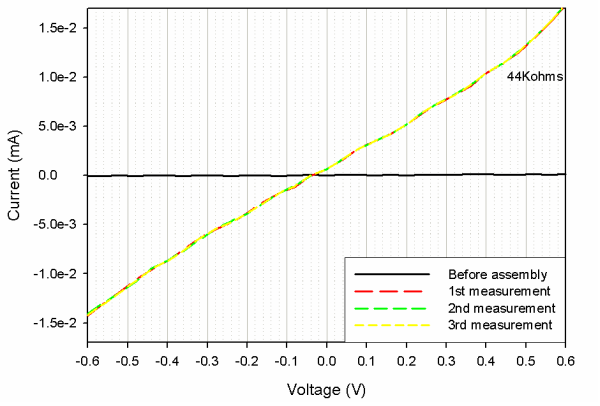

Fig. 4 Two terminal I-V measurements from assembled SWNTs.

terminal I-V measurements confirmed the connectivity between the two electrodes. Fig.4 shows two terminal I-V measurements taken after the DEP assembly process.

After DEP assembly, the SWNTs were attached to the metal electrodes with weak van der Waals forces, and also this attachment was made between two dissimilar materials. In order to address the contact problem, one approach is to utilize a focused ion beam (FIB) tool to selectively deposit metal patches on to areas where the the SWNTs are attached to the metal electrodes. In this work, we deposited a thin parylene-C layer (1µm) after the DEP assembly. The parylene coating as demonstrated previously, helped to stabilize the contact resistance between the SWNTs and the metal electrodes [24]. The black line in Fig.4 shows the I-V measurement before the DEP assembly and as expected, depicts zero net current flow. Red, green and yellow lines in Fig.4 show a sequence of stable I-V measurements after the parylene-C deposition corresponding to a measured resistance of ~ 44K Ohms.

B. CMOS Readout Circuitry

The assembly electrodes were realized using the metal 3 layer of the CMOS technology and were connected to a high gain Miller-compensated single-ended operational amplifier [25]. The SWNTs were assembled onto the feedback path of an inverting amplifier configuration (R_{ref}) as shown in Fig.5.

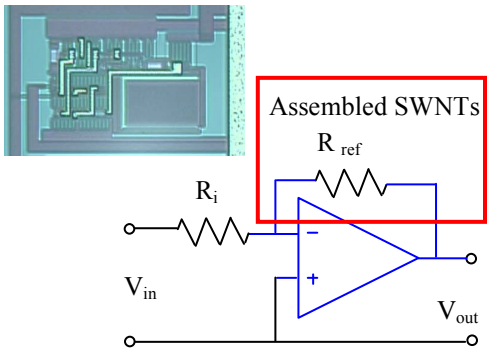

Fig.5 Schematic drawing showing an op-amp in the inverting configuration with assembled SWNTs acting as the reference resistor. Inset shows optical photograph of the fabricated op-amp.

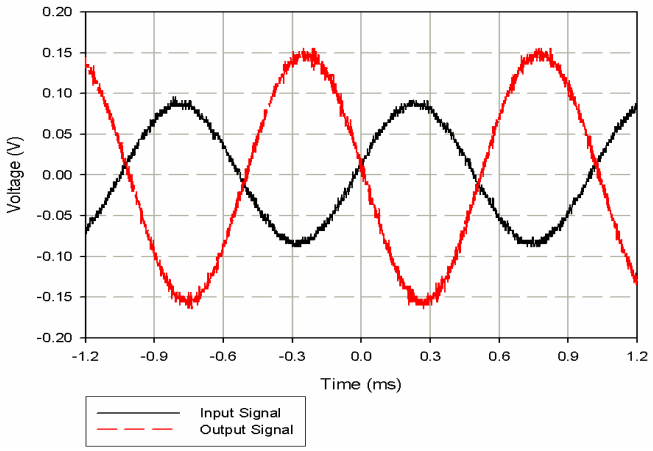

Fig. 6 Measured input and output signals from the inverting op-amp with SWNTs as the reference resistor. Using an input resistance (R_i) of 22K Ohm, the measured output gain was ~ 1.95.

The resistance of the assembled SWNTs was measured as ~44K Ohms and an external resistor (R_i) of 22K Ohms was used in the circuit. Measured input and output signals from the inverting op-amp with SWNTs as the reference resistor is displayed in Fig.6 and the gain of the inverting amplifier was measured as ~ -1.95. This value agreed well with the calculated gain (Gain=-R_{ref}/R_i = -2).

The output waveform corresponding to a unit step function was fed in to the operational amplifier with the bundled SWNTs placed as the feedback resistor is shown in Fig.7. Using the approximate relationship between the time constant and cutoff frequency [26, 27]:

$$f_c = 1/1.5t_c \qquad (1)$$

where f_c is the cutoff frequency and t_c is the time constant of the response and the cutoff frequency of the system was estimated to be ~9.5 kHz.

IV. CONCLUSIONS

Low temperature heterogeneous integration of SWNTs on to standard CMOS circuitry utilizing DEP assembly has been demonstrated. A high gain Miller-compensated single-ended

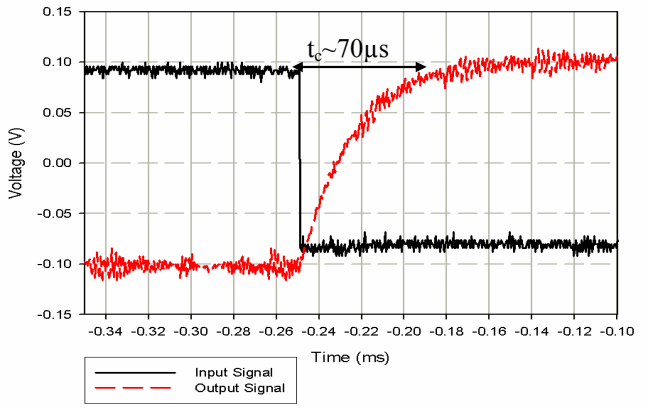

Fig. 7 Frequency response from the inverting op-amp with SWNTs as the reference resistor. The cutoff frequency was estimated to be 9.5 KHz.

operational amplifier was designed and fabricated using the AMI 0.5µm CMOS process. Electroless zincation was utilized to clean and remetallize a Zinc layer on to the Aluminum assembly electrodes. The DEP assembly was optimized (an AC signal of $5V_{pp}$ and 10MHz) to be compatible with CMOS technology. A conformal, 1µm thick parylene-C layer was deposited as an encapsulation layer to provide environmental protection and to stabilize the SWNT to metal electrode contacts. The measured two-terminal resistance of the SWNTs were around 44K Ohms. The cutoff frequency of the SWNT assembled op-amp circuit was estimated to be 9.5 KHz. This versatile approach can be extended to the integration of other nanostructures on to CMOS electronics paving way for the realization of next generation of biological and chemical nanosensors and high performance integrated circuits.

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